

REMARKS

Claims 1-8 and 10 are pending in this application. Claims 1-8 and 10 were rejected. Claims 4, 7, and 10 have been amended. Examiner's reconsideration of the rejection is respectfully requested in view of the above amendment and the following remarks.

Rejections under 35 U.S.C. § 112:

Claim 4 stands rejected under 35 U.S.C. § 112, second paragraph, for the reasons set forth on page 2 of the Office Action. Applicant has amended claim 4. Therefore, withdrawal of the rejection under 35 U.S.C. § 112, second paragraph, is requested.

Rejections under 35 U.S.C. § 102:

Claims 7-8 and 10 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,062,084 to Tomoyoshi for the reasons stated on pages 2 and 3 of the Office Action.

At the very minimum, claims 7 and 10 are believed to be patently distinct over Tomoyoshi. Indeed, at the very least, Tomoyoshi does not disclose or suggest *a position compensator for performing wafer centering*, as essentially claimed in claim 7. Furthermore, Tomoyoshi does not disclose or suggest *the process of determining the position of the wafer by examining light received by the photodetector*, as essentially claimed in claim 10.

Examiner relies on Tomoyoshi as disclosing a sensor body comprising a position compensator (30). However, applicants respectfully assert that Examiner's reliance on Tomoyoshi in this regard, is misplaced.

Tomoyoshi is directed to a deficit detection device and discloses a deficit detection unit (30). (See paragraphs 0018 and 0024). Tomoyoshi does not disclose that the deficit detection unit (30) is a *position compensator for performing wafer centering*, as essentially claimed in claim 7. In contrast, the deficit detection unit (30) in Tomoyoshi detects chipping of the substrate. (See Abstract). The deficit detection unit (30) does not detect the position of the wafer, much less perform wafer centering by determining the position of the wafer. In Tomoyoshi, the deficit unit (30) detects chipping of the substrate by the strength of the signal, but cannot recognize a position deviation, which can be solved by wafer centering provided by the claimed invention.

Furthermore, Tomoyoshi does not disclose or suggest *the process of determining the position of the wafer by examining light received by the photodetector*, as essentially claimed in claim 10 as the same reason provided for claim 7. Again, in contrast, Tomoyoshi only discloses using light and photodetectors to detect chippings of the substrate.

Accordingly, Tomoyoshi does not anticipate claims 7 and 10. Claim 8 depends from claim 7. The dependent claim 8 is believed to be allowable due to its dependency on the allowable independent claim. The Examiner's reconsideration of the rejection is respectfully requested.

Rejections under 35 U.S.C. § 103:

Claims 1-6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tomoyoshi for the reasons stated on pages 3-4 of the Office Action. The rejection is respectfully traversed.

Claim 1 is directed to a multi-functioned wafer aligner comprising a multi-functioned unit and a processor. The processor of claim 1 *determines positions of wafer centering and wafer flat zone alignment, and wafer damage by calculating an accumulated digital signal.*

Examiner stated that “it is notoriously well known in the art to center a wafer before rotating and detect a flat zone for alignment purposes. Further, it is well known that digital processors are more robust to noise than analog devices.”

Applicant respectfully submits that Tomoyoshi does not suggest wafer centering for at least the same reasons given above for claims 7 and 10. In Tomoyoshi, the deficit unit (30) detects chipping of the substrate by the strength of the signal, but cannot recognize a position deviation, which can be solved by wafer centering of the present invention. Thus, Tomoyoshi would not motivate one of ordinary skill in the art to center the wafer during the wafer damage detection.

Furthermore, the noticed facts by Examiner should not be considered to be well-known in the art because Tomoyoshi does not suggest that the analog detector would be replaced by a digital processor. In contrast, Tomoyoshi emphasizes the importance of the analog method by stating that “it cannot be overemphasized that it is possible to judge the existence of a chipping also by detecting the change of state of the scattered light under detection actuation, i.e., *a change of a signal on the strength.* By doing this, it becomes unnecessary to set up predetermined signal strength beforehand, and *improvement in the speed of the further processing can be attained.*” (See paragraph 0023). Tomoyoshi emphasizes the importance of the analog method based upon the change of the signal strength. Thus, Tomoyoshi would not motivate one of ordinary skill in the art to change the analog method to the digital method.

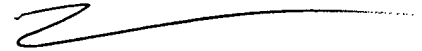
Accordingly, claim 1 is believed to be patently distinguished and not rendered obvious by Tomoyoshi. The Examiner's reconsideration is respectfully requested.

Claims 2-6 depend from claim 1. The dependent claims are believed to be allowable due to their dependency on the allowable independent claim.

Conclusion

For the foregoing reasons, the present application, including claims 1-8 and 10, is believed to be in condition for allowance. The Examiner's early and favorable action is respectfully requested. The Examiner is invited to contact the undersigned if he has any questions or comments in this matter.

Respectfully submitted,



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